CLAIMS:

1. Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, characterized in that switching means operate the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from a block of line pointers in address table register means with the output of pixel counting means, and in a second mode wherein a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means.

2. Driving circuit for a display system comprising a memory for video data to be displayed and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory, characterized in that the memory contains a full table of line pointers, each line pointer being part of a memory address for video data, and in that the address sequencer is provided with address table register means for a block of line pointers from said table of line pointers, means for successively updating the address table register means with subsequent blocks of line pointers, and pixel counting means, the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data.

3. Driving circuit as claimed in claim 2, characterized in that switching means are provided by which alternately memory addresses for video data are generated in a first mode in the address sequencer, and in a second mode the address table register is updated with a next block of line pointers.

4. Driving circuit as claimed in claim 2 or 3, characterized in that the memory comprises a full table of line pointers for different sequences of video data to be displayed.

5. Apparatus for displaying images comprising a display system and a driving circuit according to any one of the claims 2 to 4.

6. Algorithm for processing addresses in a driving circuit for a display system according to any one of the claims 2 to 4 and in the apparatus according to claim 5.

7. Computer program capable of running on signal processing means in a driving circuit for a display system according to any one of the claims 2 to 4 or in the apparatus according to claim 5.

8. Information carrier containing the computer program according to claim 7.